CoolMOS™ Power Transistor

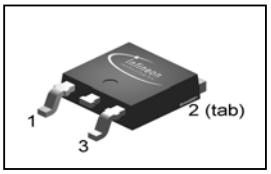
Features

- Lowest figure of merit R_{ON} x Q_g
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Pb-free lead plating; RoHS compliant
- Quailfied according to JEDEC[1)] for target applications

Product Summary

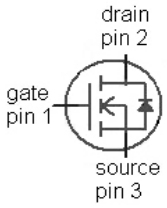
V_{DS} @T_{jmax}	550	V
$R_{DS(on),max}$	0.399	Ω
$Q_{g,typ}$	17	nC

PG-TO252



CoolMOS CP is designed for:

- Hard and softswitching SMPS topologies
- DCM PFC for Lamp Ballast
- PWM for Lamp Ballast & PDP and LCD TV



Type	Package	Marking
IPD50R399CP	PG-TO252	5R399CP

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	9	A
		T_C=100 °C	6	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C	20	
Avalanche energy, single pulse	E_{AS}	I_D=3.3 A, V_{DD}=50 V	215	mJ
Avalanche energy, repetitive t_{AR}[2),3)]	E_{AR}	I_D=3.3 A, V_{DD}=50 V	0.33	
Avalanche current, repetitive t_{AR}[2),3)]	I_{AR}		3.3	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=0...400 V	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
		AC (f>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	83	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current	I_S	T_C=25 °C	4.9	A
Diode pulse current[2]	$I_{S,pulse}$		20	
Reverse diode dv/dt[4]	dv/dt		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.5	K/W
Thermal resistance, junction - ambient	R_{thJA}	leaded	-	-	62	
Soldering temperature, reflowsoldering	T_{sold}	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250 µA	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.33 mA	2.5	3	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=500 V, V_{GS}=0 V, T_j=25 °C	-	-	1	µA
		V_{DS}=500 V, V_{GS}=0 V, T_j=150 °C	-	10	-	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=4.9 A, T_j=25 °C	-	0.36	0.399	Ω
		V_{GS}=10 V, I_D=4.9 A, T_j=150 °C	-	0.90	-	
Gate resistance	R_G	f=1 MHz, open drain	-	2.2	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz	-	890	-	pF
Output capacitance	C_{oss}		-	40	-	
Effective output capacitance, energy related[6]	$C_{o(er)}$	V_{GS}=0 V, V_{DS}=0 V to 400 V	-	38	-	
Effective output capacitance, time related[7]	$C_{o(tr)}$		-	81	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=400 V, V_{GS}=10 V, I_D=4.9 A, R_G=35.1 Ω	-	35	-	ns
Rise time	t_r		-	14	-	
Turn-off delay time	$t_{d(off)}$		-	80	-	
Fall time	t_f		-	14	-	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=400 V, I_D=4.9 A, V_{GS}=0 to 10 V	-	4	-	nC
Gate to drain charge	Q_{gd}		-	6	-	
Gate charge total	Q_g		-	17	23	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V
Reverse Diode						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=4.9 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_R=400 V, I_F=I_S, di_F/dt=100 A/µs	-	260	-	ns
Reverse recovery charge	Q_{rr}		-	1.9	-	µC
Peak reverse recovery current	I_{rrm}		-	12.2	-	A

[1] J-STD20 and JESD22

[2] Pulse width t_p limited by $T_{j,max}$

[3] Repetitive avalanche causes additional power losses that can be calculated as P_{AV}=E_{AR}*f.

[4] I_{SD}≤I_D, di/dt≤400A/µs, V_{DClink}=400V, V_{peak}<$V_{(BR)DSS}$, T_j<T_{jmax}, identical low and high side switch

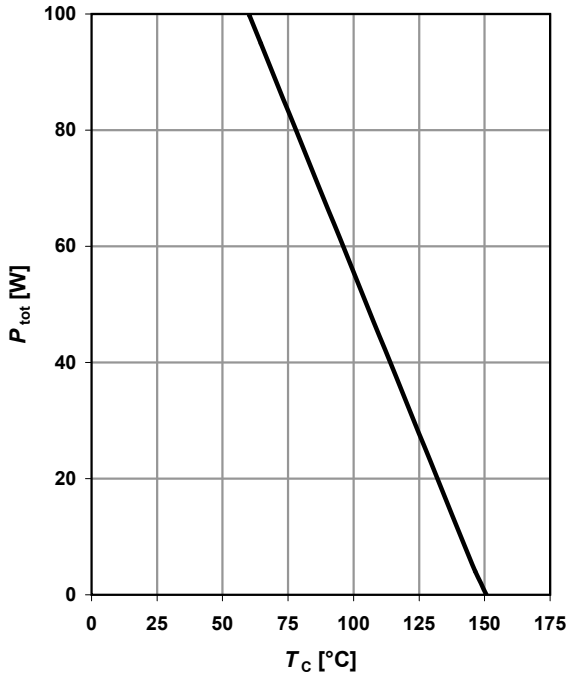
[5] Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm2 (one layer, 70mm thick) copper area for drain connection. PCB without blown air.

[6] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[7] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

1 Power dissipation

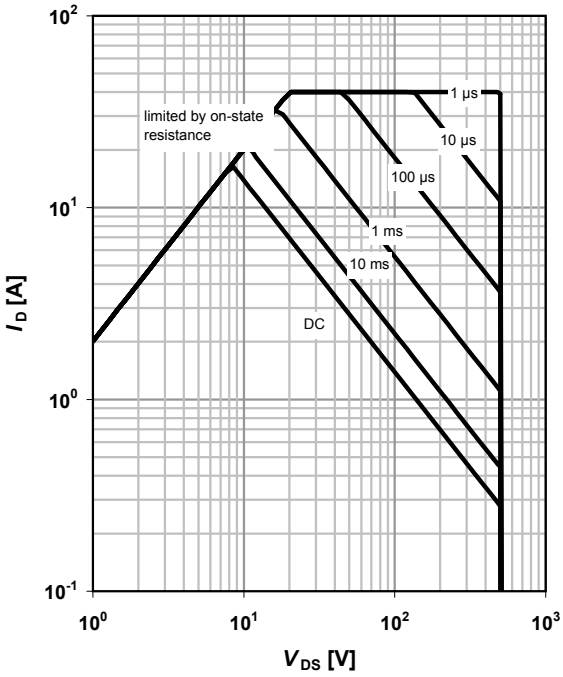
$P_{tot}=f(T_C)$



2 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

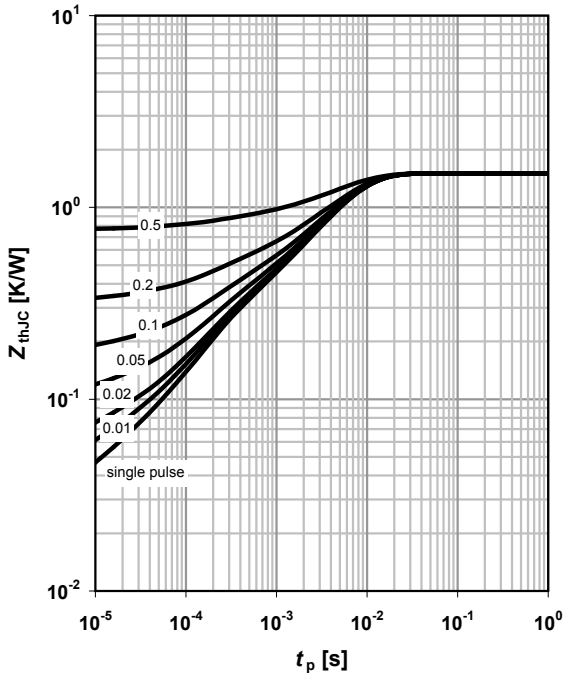
parameter: t_p



3 Max. transient thermal impedance

$Z_{(thJC)}=f(t_p)$;

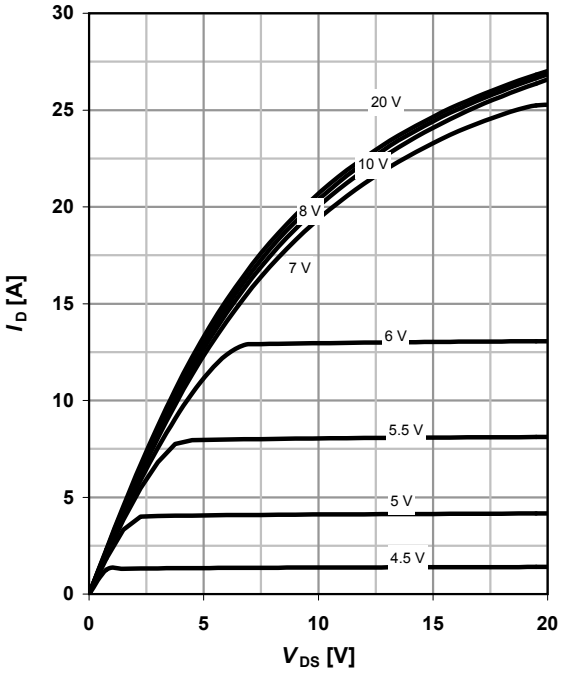
parameter: $D=t_p/T$



4 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

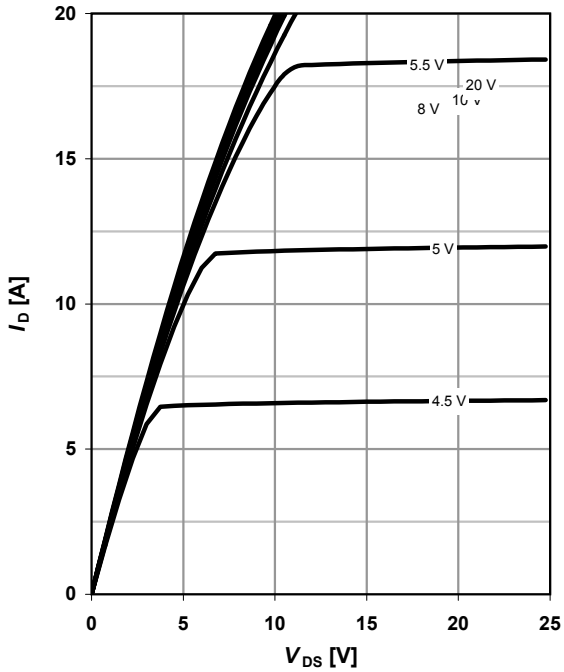
parameter: V_{GS}



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=150 °C

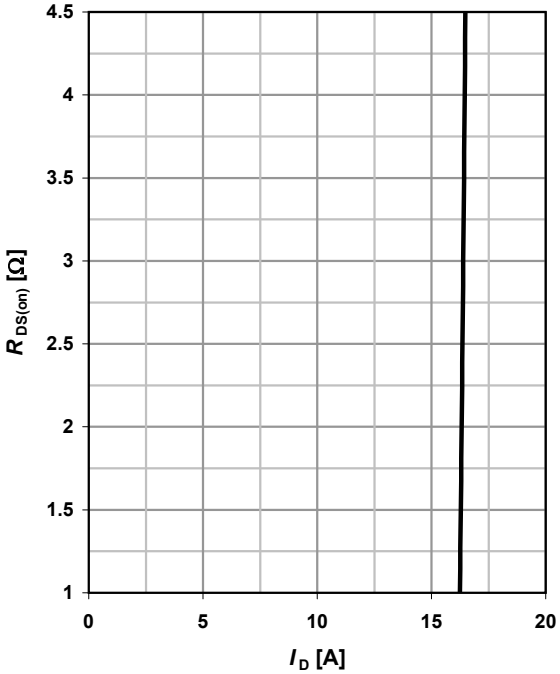
parameter: V_{GS}



6 Typ. drain-source on-state resistance

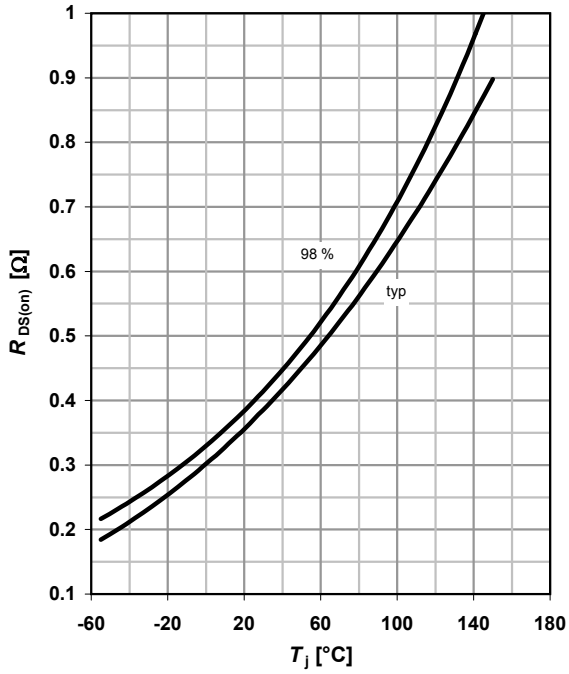
$R_{DS(on)}$=f(I_D); T_j=150 °C

parameter: V_{GS}



7 Drain-source on-state resistance

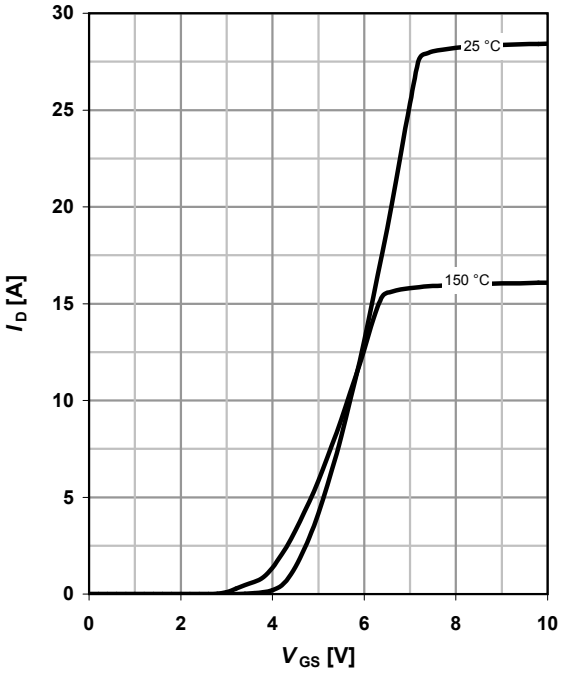
$R_{DS(on)}$=f(T_j); I_D=4.9 A; V_{GS}=10 V



8 Typ. transfer characteristics

I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

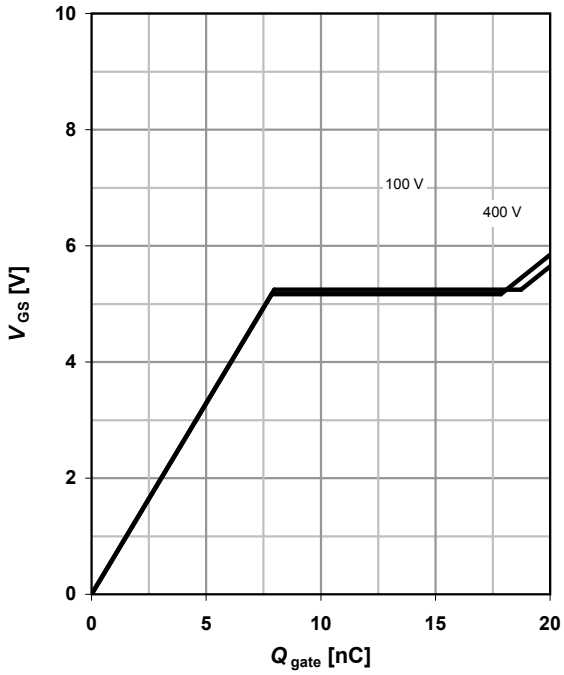
parameter: T_j



9 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=4.9 A pulsed

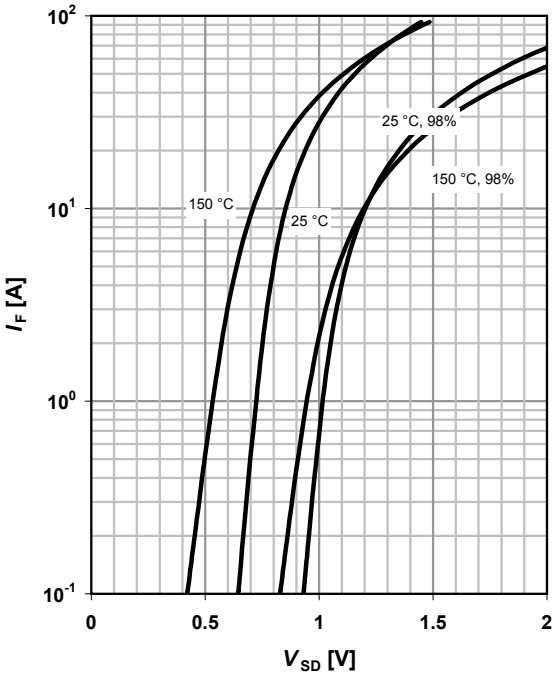
parameter: V_{DD}



10 Forward characteristics of reverse diode

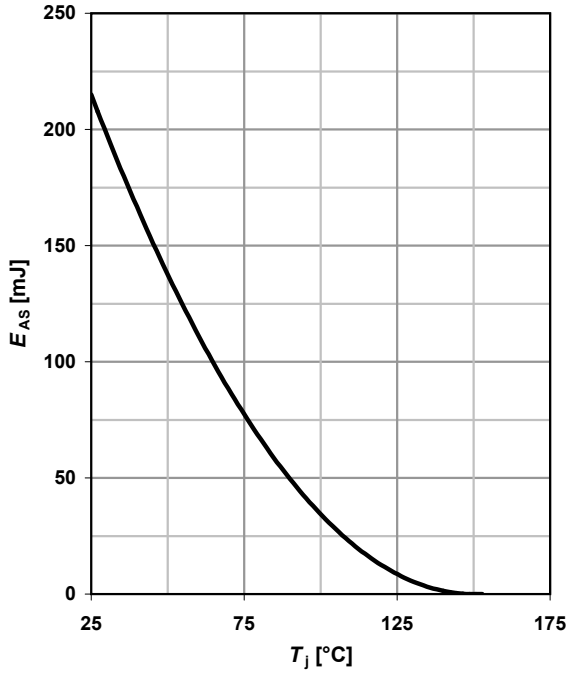
I_F=f(V_{SD})

parameter: T_j



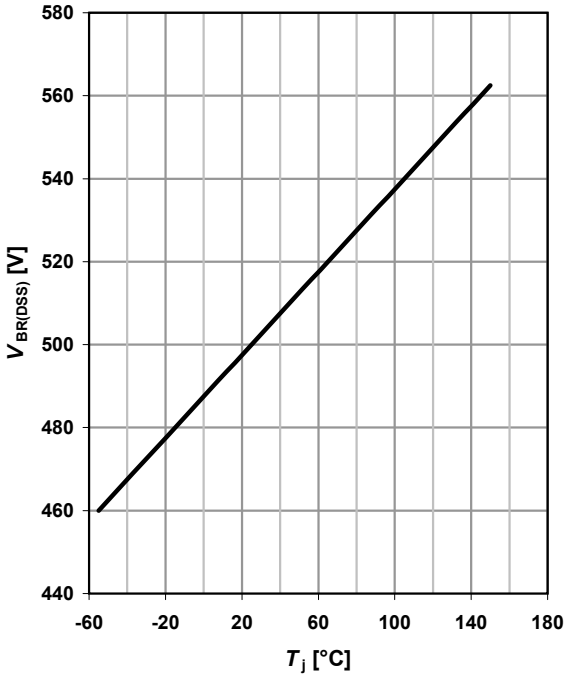
11 Avalanche energy

E_{AS}=f(T_j); I_D=3.3 A; V_{DD}=50 V



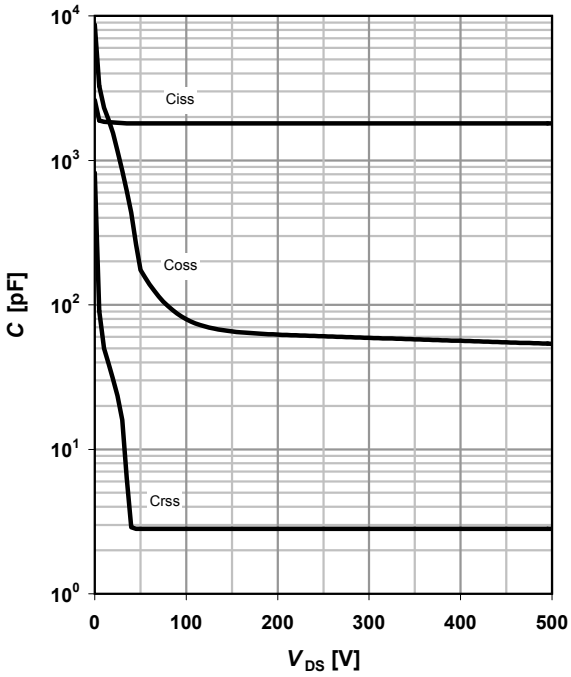
12 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA



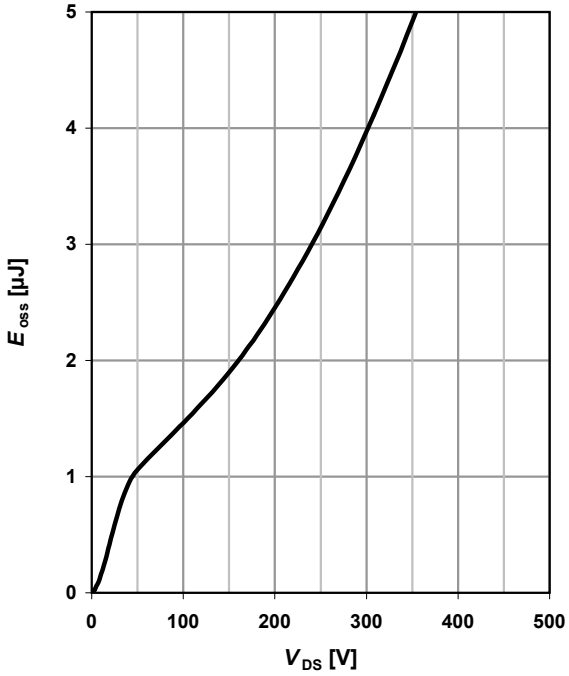
13 Typ. capacitances

C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

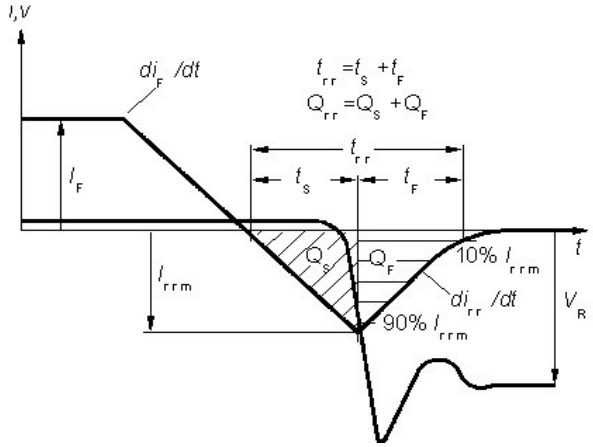


14 Typ. Coss stored energy

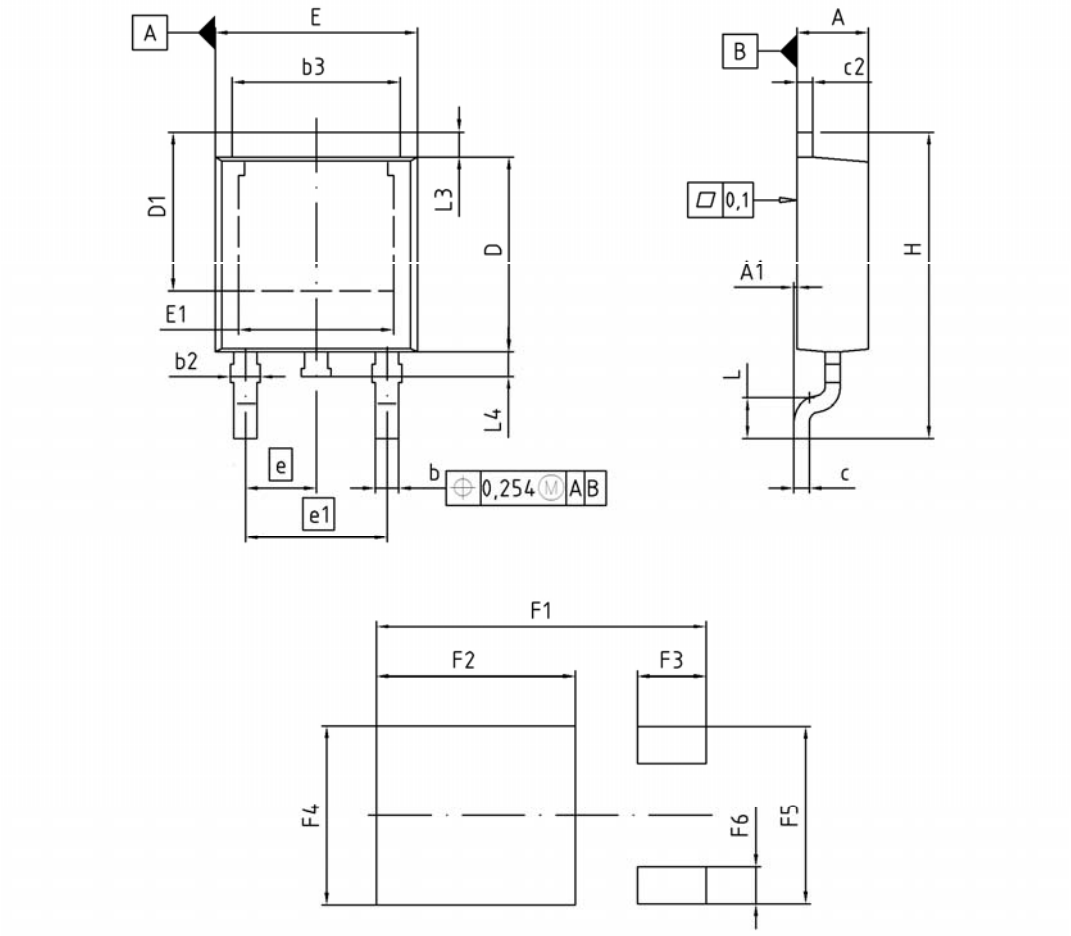
E_{oss}=f(V_{DS})



Definition of diode switching characteristics



PG-TO252-3-1/PG-TO252-3-11/PG-TO252-3-21: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051

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